What is claimed is:

1. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:

coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;

coupling the bit line and the input node to a first potential node to receive a precharge potential;

applying a reference current to the input node;

driving a word line coupled to a control gate of the floating-gate memory cell;

isolating the bit line and the input node from the first potential node; and

sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

2. The method of claim 1, wherein applying a reference current to the input node comprises:

generating a reference current, wherein the reference current varies inversely with changes in ambient temperature; and

applying the reference current to the input node.

3. The method of claim 1, wherein applying a reference current to the input node comprises:

generating a reference current control signal having a potential level, wherein the potential level of the reference current control signal varies proportionately with changes in ambient temperature;

generating a reference current in response to the potential level of the reference current control signal, wherein the reference current varies inversely with the changes in ambient temperature; and

applying the reference current to the input node.

4. The method of claim 1, wherein applying a reference current to the input node comprises:

generating a reference current control signal having a potential level, wherein the reference current control signal is generated at an output node located at an output of a diode having an input coupled to receive a supply potential from a second potential node, and wherein a resistive component is coupled between the output node and a third potential node coupled to receive a ground potential;

generating a reference current in response to the potential level of the reference current control signal; and

applying the reference current to the input node.

5. The method of claim 1, wherein applying a reference current to the input node comprises:

generating a reference current control signal having a potential level, wherein the reference current control signal is generated at an output node located at an output of an array of diode-connected p-channel field-effect transistors each having a first source/drain region coupled to receive a supply potential from a second potential node, a second source/drain region coupled to the output node and a gate coupled to the output node, wherein a resistive component is coupled between the output node and a third potential node coupled to receive a ground potential, and wherein a first n-channel field-effect transistor and a second n-channel field-effect transistor are coupled in series between the output node and the resistive component; and

applying the reference current control signal to a gate of a p-channel field-effect transistor coupled between the input node and a fourth potential node coupled to receive the supply potential, thereby applying the reference current to the input node.

6. The method of claim 5, wherein the resistive component comprises:
a first resistive element coupled between the third potential node and the output node; and
a first field-effect transistor coupled between the first resistive element and the third potential node and responsive to a first control signal.

7. The method of claim 6, wherein the resistive component further comprises:
a second resistive element coupled in parallel with the first resistive element between the third potential node and the output node; and
a second field-effect transistor coupled between the second resistive element and the third potential node and responsive to a second control signal different from the first control signal.

8. The method of claim 7, wherein the resistive component further comprises:
at least one additional resistive element coupled in parallel with the first resistive element between the third potential node and the output node; and
at least one additional field-effect transistor, each additional field-effect transistor coupled between one of the additional resistive elements and the third potential node and each additional field-effect transistor responsive to an additional control signal different from the first control signal.

9. The method of claim 5, wherein the resistive component comprises a plurality of resistive elements selectively coupled in parallel between the third potential node and the output node.

10. The method of claim 5, wherein each p-channel field-effect transistor is sized to be substantially identical to the p-channel field-effect transistor.

11. The method of claim 5, wherein the first n-channel field-effect transistor is sized to be substantially identical to a first pass transistor coupled between the floating-gate

memory cell and the input node and the second n-channel field-effect transistor is sized to be substantially identical to a second pass transistor coupled between the floating-gate memory cell and the input node.

12. The method of claim 1, wherein the reference current is less than one-half an expected current flow through the floating-gate memory cell in an erased state.

13. The method of claim 1, wherein the reference current is approximately one order of magnitude less than an expected current flow through the floating-gate memory cell in an erased state.

14. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:

coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;

coupling the bit line and the input node to a first potential node to receive a precharge potential;

generating a reference current, wherein the reference current varies inversely with changes in ambient temperature and wherein the reference current is less than one-half an expected current flow through the floating-gate memory cell in an erased state;

applying the reference current to the input node;

driving a word line coupled to a control gate of the floating-gate memory cell;

isolating the bit line and the input node from the first potential node; and

sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

15. The method of claim 14, wherein the reference current is approximately one order of magnitude less than the expected current flow through the floating-gate memory cell in the erased state.

16. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:

coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;

coupling the bit line and the input node to a first potential node to receive a precharge potential;

generating a reference current control signal having a potential level, wherein the potential level of the reference current control signal varies proportionately with changes in ambient temperature;

generating a reference current in response to the potential level of the reference current control signal, wherein the reference current varies inversely with the changes in ambient temperature and wherein the reference current is less than one-half an expected current flow through the floating-gate memory cell in an erased state;

applying the reference current to the input node;

driving a word line coupled to a control gate of the floating-gate memory cell;

isolating the bit line and the input node from the first potential node; and

sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

17. The method of claim 16, wherein the reference current is approximately one order of magnitude less than the expected current flow through the floating-gate memory cell in the erased state.

18. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:

coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;

coupling the bit line and the input node to a first potential node to receive a precharge potential;

generating a reference current control signal having a potential level, wherein the potential level of the reference current control signal varies proportionately with changes in ambient temperature;

generating a reference current in response to the potential level of the reference current control signal, wherein the reference current varies inversely with the changes in ambient temperature and is less than one-half an expected current flow through the floating-gate memory cell in an erased state;

applying the reference current to the input node;

driving a word line coupled to a control gate of the floating-gate memory cell;

isolating the bit line and the input node from the first potential node; and

sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

19. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:

coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;

coupling the bit line and the input node to a first potential node to receive a precharge potential;

generating a reference current, wherein the reference current varies inversely with changes in ambient temperature and is less than one-half an expected current flow through the floating-gate memory cell in an erased state;

applying the reference current to the input node;

driving a word line coupled to a control gate of the floating-gate memory cell;
isolating the bit line and the input node from the first potential node; and
sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

20. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:
coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;
coupling the bit line and the input node to a first potential node to receive a precharge potential;
generating a reference current control signal having a potential level, wherein the reference current control signal is generated at an output node located at an output of a diode having an input coupled to receive a supply potential from a second potential node, and wherein a resistive component is coupled between the output node and a third potential node coupled to receive a ground potential;
generating a reference current in response to the potential level of the reference current control signal, wherein the reference current is less than one-half an expected current flow through the floating-gate memory cell in an erased state;
applying the reference current to the input node;
driving a word line coupled to a control gate of the floating-gate memory cell;
isolating the bit line and the input node from the first potential node; and
sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

21. A method of sensing a programmed state of a floating-gate memory cell, the method comprising:

coupling a bit line to an input node of a single-ended sensing device, wherein the bit line is coupled to a source/drain region of the floating-gate memory cell;

coupling the bit line and the input node to a first potential node to receive a precharge potential;

generating a reference current control signal having a potential level, wherein the reference current control signal is generated at an output node located at an output of an array of diode-connected p-channel field-effect transistors each having a first source/drain region coupled to receive a supply potential from a second potential node, a second source/drain region coupled to the output node and a gate coupled to the output node, wherein a resistive component is coupled between the output node and a third potential node coupled to receive a ground potential, and wherein a first n-channel field-effect transistor and a second n-channel field-effect transistor are coupled in series between the output node and the resistive component;

applying the reference current control signal to a gate of a p-channel field-effect transistor coupled between the input node and a fourth potential node coupled to receive the supply potential, thereby applying the reference current to the input node, wherein the reference current is less than one-half an expected current flow through the floating-gate memory cell in an erased state;

driving a word line coupled to a control gate of the floating-gate memory cell;

isolating the bit line and the input node from the first potential node; and

sensing a potential level at the input node while applying the reference current, wherein the potential level at the input node is indicative of the programmed state of the floating-gate memory cell.

22. The method of claim 21, wherein the resistive component comprises:

a first resistive element coupled between the third potential node and the output node;

a first field-effect transistor coupled between the first resistive element and the third potential node and responsive to a first control signal;

a second resistive element coupled in parallel with the first resistive element between the third potential node and the output node; and

a second field-effect transistor coupled between the second resistive element and the third potential node and responsive to a second control signal different from the first control signal.

23. The method of claim 22, wherein the resistive component further comprises:

at least one additional resistive element coupled in parallel with the first resistive element between the third potential node and the output node; and

at least one additional field-effect transistor, each additional field-effect transistor coupled between one of the additional resistive elements and the third potential node and each additional field-effect transistor responsive to an additional control signal different from the first control signal.

24. The method of claim 21, further comprising:

wherein each diode-connected p-channel field-effect transistor is sized to be substantially identical to the p-channel field-effect transistor coupled between the input node and a fourth potential node; and

wherein the first n-channel field-effect transistor is sized to be substantially identical to a first pass transistor coupled between the floating-gate memory cell and the input node and the second n-channel field-effect transistor is sized to be substantially identical to a second pass transistor coupled between the floating-gate memory cell and the input node.